93

RCE 2800

PTO/SB/30 (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Commissioner for Patents
Box RCE
Washington DC 20231

Application Number	09/990,330
Filing Date	November 21, 2001
First Named Inventor	James D. Beasom
Art Unit	2814
Examiner Name	Howard Weiss
Attorney Docket Number	125.009US01

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114

a. [X] Previously submitted
   i. [ ] Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on _____
   (Any unentered amendment(s) referred to above will be entered).
   ii. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
   iii. [X] Other Copy of Supplemental Information Disclosure Statement, Form 1449, copy of International Search Report, and copies of 5 documents previously filed on May 19, 2003 (Exhibit A); Communication Regarding Uninitialed 1449 previously filed on September 22, 2003 (Exhibit B)

b. [X] Enclosed
   i. [ ] Amendment/Response (__ pgs.)
   ii. [ ] Affidavit(s)/Declaration(s)
   iii. [ ] Information Disclosure Statement (IDS)
   iv. [X] Other: Second Communication Regarding Uninitialed 1449 (3 pgs.)

2. Miscellaneous

a. [ ] Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

b. [ ] Other _____

3. Fees — The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

a. [X] The Director is hereby authorized to charge any additional fees, or credit any overpayments, to Deposit Account No. 502432
   i. [ ] RCE fee of $770.00 required under 37 CFR 1.17(e)
   ii. [ ] One-Month Extension of time fee of $110.00 (37 CFR 1.136 and 1.17)
   iii. [ ] Other: Petition Fee of $130.00

b. [X] Payment by credit card for $ 770 is enclosed for the RCE fee.

c. [ ] Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Scott V. Lundberg	Registration No. (Attorney/Agent)	41,958
Signature		Date	October 8, 2003

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being mailed to the United States Patent and Trademark Office via first class mail addressed to: Mail Stop RCE, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.:

Name (Print/Type)	Jane E. Sagers	Date	October 8, 2003
Signature			

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND Fees and Completed Forms to the following address: Assistant Commissioner for Patents, Box RCE, Washington, DC 20231.

10/15/2003 CHBUYEN 00000064 09990330
01 FC:1801 770.00 DP

MATCH & RETURN

Applicant(s)	James D. Beasom
Serial No.	09/990,330
Filing Date	November 21, 2001
Examiner Name	Howard Weiss
Group Art Unit	2814
Allowed	July 8, 2003
Confirmation No.	2642
Attorney Docket No.	125.009US01

SECOND COMMUNICATION REGARDING UNINITIALED 1449

Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

Mail Stop Box RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant submitted a Supplemental Information Disclosure Statement, Form 1449 and copies of 5 references on May 16, 2003 in the above-referenced patent application. Subsequently, a Notice of Allowance, dated July 8, 2003, was issued. The notice of allowance did not include an initialized copy of the filed 1449. Ms. Bauer, paralegal with Fogg and Associates, discussed the omission in a telephone conversation on July 24, 2003 with Examiner Weiss. The Examiner indicated that he did not receive the Supplemental Information Disclosure Statement before allowing the case and requested that we wait a while to see it the Supplemental Information Disclosure Statement catches up with the file. Applicant waited approximately 2 months to see if a "match-up" occurred, which it did not. Applicant re-filed the Supplemental Information Disclosure Statement along with a copy of the return-receipt postcard on September 18, 2003. Ms. Bauer, spoke to Examiner Weiss on October 7, 2003 to find out whether or not he had received either of these filings and was again told that there was no record of these being received by the U.S. Patent and Trademark Office. Examiner Weiss advised us to go ahead and pay the issue fee and that he would order the file to review the 1449. Applicant's representative was not comfortable paying the issue fee without an initialized 1449, therefore, had no other choice but to file an RCE to get the art reviewed. Attached please find a copy of the following documents as outlined below:

EXHIBIT A: Supplemental Information Disclosure Statement originally filed on May 16, 2003.

(1) A copy of the return-receipt postcard listing the Supplemental Information Disclosure Statement, Form 1449, copy of International Search Report, and copies of 5 documents, which is date-stamped as being received by the U.S. Patent Office (OIPE) on May 19, 2003;

(2) The transmittal form accompanying same;

(3) Supplemental Information Disclosure Statement as filed;

(4) Form 1449 as filed; and

(5) Copies of 5 documents.

EXHIBIT B: Re-filing of the Supplemental Information Disclosure Statement on September 18, 2003.

(1) A copy of the return-receipt postcard listing the Communication Regarding Uninitialized 1449 and Exhibit A above, which is date-stamped as being received by the U.S. Patent Office (OIPE) on September 22, 2003.

(2) Communication Regarding Uninitialized 1559;

(3) The transmittal form accompanying same;

(4) Supplemental Information Disclosure Statement as filed;

(5) Form 1449 as filed.

(6) Copies of 5 documents [see Exhibit A No. (5)]

Applicant respectfully requests that this Supplemental Information Disclosure Statement, as filed on May 16, 2003, be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP §609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant.

It is believed that no fee is due; however, should fees be required, the Commissioner for Patents is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. 502432.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

Date: 10-8-03

Scott V. Lundberg
Reg. No. 41,958

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T – (612) 332-4720
F – (612) 677-3553

Exhibit A

Receipt of the below-listed documents is hereby acknowledged in the U.S. Patent and Trademark Office:

Applicant:	James D. Beasom
Serial No.:	09/990,330
Filing date:	November 21, 2001
Title:	A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

Enclosed: A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), copy of International Search Report and copies of 5 documents; and transmittal document.

Mailed via First Class Mail: May 16, 2003
Attorney Docket No.: 125.009US01
SVL:eab

Receipt of the below-listed documents is hereby acknowledged in the U.S. Patent and Trademark Office:

Applicant:	James D. Beasom
Serial No.:	09/990,330
Filing date:	November 21, 2001
Title:	A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

Enclosed: A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), copy of International Search Report and copies of 5 documents; and transmittal document.

Mailed via First Class Mail: May 16, 2003
Attorney Docket No.: 125.009US01
SVL:eab

Applicant(s)	James D. Beasom	TRANSMITTAL FORM UNDER 37 CFR 1.8 (LARGE ENTITY)
Serial No.	09/990,330	
Filing Date	November 21, 2001	
Group Art Unit	2814	
Examiner Name	Howard Weiss	
Confirmation No.	6841	
Attorney Docket No.	125.009US01	
Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Enclosures

The following documents are enclosed:

X Supplemental Information Disclosure Statement (2 pgs.); Form 1449 (1 pg.); copy of International Search Report, and copies of 5 documents.
X A return postcard.

Please charge any additional fees or credit any overpayments to Deposit Account No. 502432.

CUSTOMER NO. 34206

Submitted By

Name	Scott V. Lundberg	Reg. No.	41,958	Telephone	(612) 332-4720
Signature				Date	May 6, 2003

Attorneys for Applicant
Fogg & Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T: 612-332-4720
F: 612-677-3553

Certificate of Mailing

I certify that this correspondence, and the documents identified above, are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 6, 2003.

Name	Elizabeth A. Bauer	Signature	Elizabeth A. Bauer

Applicant(s)	James D. Beasom	SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
Serial No.	09/990,330	
Filing Date	November 21, 2001	
Group Art Unit	2814	
Examiner	Howard Weiss	
Attorney Docket No.	125.009US01	
Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with 37 C.F.R. §§ 1.56 and 1.97, *et seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified Application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the references listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to MPEP §609, Applicant further requests that the Examiner initial next to each reference on the Form 1449 to indicate that the listed references have been considered. Applicant further requests that a copy of the initialed Form 1449 be returned with the next official communication.

The enclosed references were recently cited in a communication in a counterpart foreign application. A copy of the International Search Report is enclosed herewith.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

CERTIFICATION UNDER 37 CFR 1.97(e)(1)

The undersigned attorney hereby certifies that each item of information contained in this Supplemental Information Disclosure Statement was cited in a communication form a foreign patent office in a counterpart foreign application as indicated above, not

more than three months prior to the mailing date of this Supplemental Information Disclosure Statement.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the number listed below.

Respectfully submitted,

Date: 5-16-03

Scott V. Lundberg
Reg. No. 41,958

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T: 612-332-4720
F: 612-677-3553

Applicant(s)	...es D. Beasom
Serial No.	09/990,330
Filing Date	November 21, 2001
Group Art Unit	2814
Examiner Name	Howard Weiss
Attorney Docket No.	125.009US01

INFORMATION DISCLOSURE STATEMENT FORM PTO-1449

Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

U.S. Patent References

Examiner Initials	Patent No.	Issue Date	Name	Filing Date
	5,264,719	11/23/93	Beasom	05/24/91
	5,482,888	01/09/96	Hsu et al.	08/12/94
	5,918,137	06/29/99	Ng et al.	04/27/98

Foreign Patent References

Examiner Initials	Foreign Patent		Name	Publication Date	T
	Country	No.			
	EP	0309828		04/05/89	
	GB	2215515		09/20/89	

Other References

Examiner Initials	Author, Title, Date, Pages, etc.
	NONE

Examiner Signature		Date Considered	

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Receipt of the below-listed documents is hereby acknowledged in the U.S. Patent and Trademark Office:

Applicant: James D. Beasom
Serial No.: 09/990,330
[illegible] 21, 2001

Receipt of the below-listed documents is hereby acknowledged in the U.S. Patent and Trademark Office:

Applicant: James D. Beasom
Serial No.: 09/990,330
Filing date: November 21, 2001
Allowed: July 8, 2003
Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

Enclosed: Communication Regarding Uninitialed 1449 (2 pgs.) and Exhibit A (which includes copies of return receipt postcard, copy of International Search Report, Supplemental Information Disclosure Statement, Form 1449, and copies of 5 documents filed on May 16, 2003); and Transmittal document.

Exhibit B

Mailed via First Class Mail: September 18, 2003
Attorney Docket No.: 125.009US01
SVL:eab

Applicant(s)	James D. Beasom	COMMUNICATION REGARDING UNINITIALED 1449
Serial No.	09/990,330	
Filing Date	November 21, 2001	
Examiner Name	Howard Weiss	
Group Art Unit	2814	
Allowed	July 8, 2003	
Confirmation No.	2642	
Attorney Docket No.	125.009US01	
Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant submitted a Supplemental Information Disclosure Statement, Form 1449 and copies of 5 references on May 16, 2003 in the above-referenced patent application. Subsequently, a Notice of Allowance, dated July 8, 2003, was issued. The notice of allowance did not include an initialized copy of the filed 1449. Ms. Bauer, paralegal with Fogg and Associates, discussed the omission in a telephone conversation on July 24, 2003 with Examiner Weiss. The Examiner indicated that he did not receive the Supplemental Information Disclosure Statement before allowing the case and requested that we wait a while to see it the Supplemental Information Disclosure Statement catches up with the file. Applicant has waited approximately 2 months and has received no word that this match-up has occurred. Applicant has decided to re-file the Supplemental Information Disclosure Statement along with a copy of the mail receipt.

Therefore, submitted herewith is a copy of the below-identified documents as originally filed on May 16, 2003 and identified as Exhibit A:

(1) A copy of the return-receipt postcard listing the Supplemental Information Disclosure Statement, Form 1449, copy of International Search Report, and copies of 5 documents, which is date-stamped as being received by the U.S. Patent Office (OIPE) on May 19, 2003;

(2) The transmittal form accompanying same;

(3) Supplemental Information Disclosure Statement as filed;

(4) Form 1449 as filed; and

(5) Copies of 5 documents.

Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP §609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with **as soon as possible and before the Issue Fee is due on October 8, 2003**.

It is believed that no fee is due; however, should fees be required, the Commissioner for Patents is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. 502432.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

Date: 9-18-03

Scott V. Lundberg
Reg. No. 41,958

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T – (612) 332-4720
F – (612) 677-3553

Receipt of the below-listed documents is hereby acknowledged in the U.S. Patent and Trademark Office:

Applicant:	James D. Beasom
Serial No.:	09/990,330
Filing date:	November 21, 2001
Title:	A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

Enclosed: A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), copy of International Search Report and copies of 5 documents; and transmittal document.

Mailed via First Class Mail: May 16, 2003
Attorney Docket No.: 125.009US01
SVL:eab

Exhibit A

Applicant	Beasom
Serial No.	09/990,330
Filing Date	November 21, 2001
Group Art Unit	2814
Examiner Name	Howard Weiss
Facsimile No.	703-872-9318
Attorney Docket No.	125.009US01

FACSIMILE TRANSMITTAL FORM

Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

Total Pages: 3 (including transmittal sheet)

RECEIVED
CENTRAL FAX CENTER
OCT 3 0 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

OFFICIAL

Enclosures

The following documents are enclosed:

X A Revocation and Power of Attorney and Certificate Under 37 C.F.R. §3.73(b) (2 pgs.).

CUSTOMER NUMBER: 34206

Submitted By

Name	Scott V. Lundberg	Reg No.	41,958	Telephone	(612) 332-4720
Signature				Date	October 30, 2003

Attorneys for Applicant
Fogg & Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T: 612-332-4720
F: 612-677-3553

Certificate of Transmission

I certify that this paper, and the above-identified documents, are being transmitted by facsimile to, Examiner Dana Farahani, Group Art Unit 2814 (Facsimile No. 703-872-9318) of the United States Patent and Trademark Office on October 30, 2003.

Name	Elizabeth A. Bauer	Signature	Elizabeth A. Bauer

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Beasom	Examiner: Howard Weiss
Application No.: 09/990,330	Group Art Unit: 2814
Filed: 11/21/2001	Attorney Docket No.: 125.009US01

Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REVOCATION, POWER OF ATTORNEY AND CERTIFICATE UNDER 37 C.F.R. §3.73(b)

Please revoke any existing Power of Attorney, if any, and appoint the attorneys and/or patent agents associated with **CUSTOMER NUMBER 32095** for the above-identified patent/ application.

Please send correspondence to the following address:

Attn: Scott Lundberg
Fogg & Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339

Intersil Americas Inc., a corporation organized and existing under and by virtue of the laws of Delaware, and having an office and place of business at 675 Trade Zone Boulevard, Milpitas, CA 95035, certifies that it is:

The assignee of the entire right, title, and interest in the patent/application identified above by virtue of an assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 012320, Frame 0917.

Title: A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT HAVING SEPARATED DEVICE REGIONS

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

10/24/03
Date

Signature

Paul A. Bernkopf
Typed or Printed Name

Vice President
Title

(12) UK Patent Application (19) GB (11) 2 215 515 (13) A

(43) Date of A publication 20.09.1989

(21) Application No 8806014.0

(22) Date of filing 14.03.1988

(51) INT CL*
H01L 29/08 29/78

(52) UK CL (Edition J)
H1K KCAM KCAX K1AA1 K1CA K4C11 K4C14 K4H1A K4H1C K4H3A K9B1 K9B1A K9B4A K9D1 K9E K9F K9N2 K9P1 K9R2

(56) Documents cited
GB 1233545 A EP 0195607 A2 EP 0187016 A2 EP 0098652 A2

(58) Field of search
UK CL (Edition J) H1K KAAC KAAX KCAM KCAX
INT CL* H01L

(71) Applicant
Philips Electronic and Associated Industries Limited
(Incorporated in the United Kingdom)
Arundel Great Court, 8 Arundel Street, London, WC2R 3DT, United Kingdom

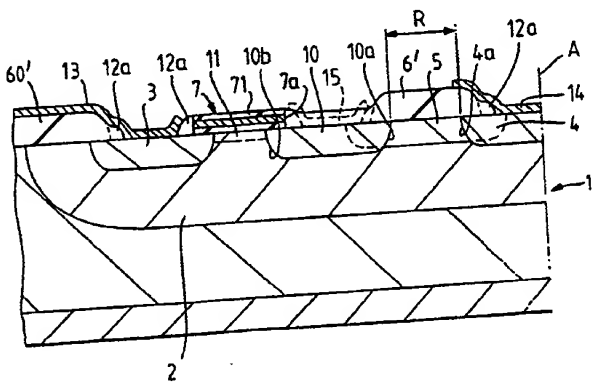
(72) Inventor
Kenneth Ronald Wright

(74) Agent and/or Address for Service
R J Boxall
Philips Electronics,
Patents and Trade Marks Department, Centre Point,
New Oxford Street, London, WC1A 1QJ,
United Kingdom

(54) A lateral insulated gate field effect transistor and a method of manufacture

(57) A transistor has a semiconductor body (1) having a first region (2) of one conductivity type adjacent a surface of the semiconductor body (1), source and drain regions (3 and 4) of the opposite conductivity type are formed spaced-apart within the first region (2) adjacent the given surface, a lowly doped extension region (5) extends beneath an insulating layer (6) on the given surface from the drain region (4) towards the source region (3), an insulated gate (7) is provided on the given surface (1a) for defining a gateable connection of the source and drain regions (3 and 4), and a further region (10) of the opposite conductivity type is provided adjacent the given surface beneath the insulating layer (6) so as to adjoin the lowly doped extension region (5) remote from the drain region (4) to define a conduction channel area (1) between the source (3) and the further region (10) beneath the insulated gate (7) so that the gateable connection of the source and drain regions is provided between the source and further regions (3 and 10). In the manufacture of the transistor, the insulated gate (7) and insulating layer (6) are used as a mask for the introduction of the impurities to form the source, drain and further regions (3, 4 and 10). Two or more further regions may be provided between the source and drain. The invention may be applied to a lateral insulated gate bipolar transistor structure.

Fig. 2.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy

GB 2 215 515 A

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 309 828**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 88115209.4

(51) Int. Cl.⁴: H01L 29/08

(22) Date of filing: 16.09.88

(30) Priority: 02.10.87 IT 2213087

(43) Date of publication of application:
05.04.89 Bulletin 89/14

(84) Designated Contracting States:
DE FR GB NL SE

(71) Applicant: SGS-THOMSON MICROELECTRONICS S.r.L.
Via C. Olivetti, 2
I-20041 Agrate Brianza Milan(IT)

(72) Inventor: Crisenza, Giuseppe Paolo
Via 11 Febbraio, 7/e
I-20056 Trezzo d'Adda Milan(IT)
Inventor: Fontana, Gabriella
Via don Tentori, 9
I-20059 Ruginello di Vimercate Milan(IT)
Inventor: Picco Paolo
Via Carlo Alberto, 39
I-20052 Monza Milan(IT)

(74) Representative: Perani, Aurelio et al
c/o JACOBACCI-CASETTA & PERANI 7, Via Visconti di Modrone
I-20122 Milano(IT)

(54) An electronic semiconductor device, in particular a silicon-gate field-effect MOS transistor, for high input voltages.

(57) An electronic semiconductor device (1), in particular a silicon-gate field-effect MOS transistor obtained from a C MOS process and adapted for high input voltages, comprises a so-called Well pocket (3) having opposite doping from that of the semiconductor substrate (2) and inside which there are formed the source (4) and drain (5) zones of the transistor, as well as a layer (5a) with opposite doping from that of the Well pocket (3) and forming a side extension of the transistor drain (5) zone and being self-aligned to the gate oxide (6a) and covered with a layer of an isolating oxide (10). That layer (5a) is doped at a lower dopant concentration than that of the drain (5) zone, and the device (1) so made can also operate at significantly higher voltages than those applicable to other components of a circuit to which it is integrated.

EP 0 309 828 A2

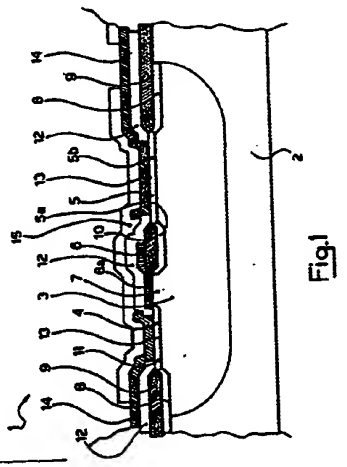


Fig.1